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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/473,305	12/28/99	FRUTSCHY K	42390-P7663

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PAREKH, N	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/473,305	Frutschy et al
Examiner	**Group Art Unit**
Nitin Parekh	2811

☒ Responsive to communication(s) filed on *Jan 2, 1901*

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1, 2, 4-7, 12-16, 23, 25, and 28-33* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1, 2, 4-7, 12-16, 23, 25, and 28-33* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 4-7, 12-16, 23, 25 and 28-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Hembree (US Pat. 5783461) and Domadia et al (US Pat. 5949137) and Akram (US Pat. 5736456).

Regarding claim 1, the APA discloses a microelectronic component assembly comprising:

- a substrate having contacts

- a motherboard having contacts

- solder balls extending between the substrate contacts and motherboard contacts and attached to one of those contacts, and

- a compression mechanism/support structure for imparting pressure between the substrate and the motherboard

(Specification- Fig. 5; pp. 1-3).

Regarding claims 2 and 4, the APA discloses the substrate comprising a microelectronic package/carrier substrate/microelectronic device.

Regarding claim 5, the APA disclose the solder balls extending between the substrate and motherboard contacts and attached to the respective contacts but fails to specify forming a recess defined by a sidewalls extending into the motherboard. Hembree teaches forming non-reflow electrical contacts between the microelectronic device and a board/substrate comprising a recess defined by inclined sidewalls of the bumps (Fig. 5; Col. 6, line 34-65) or vertical sidewalls (Fig. 5A; Col. 6, line 34-65) extending into the board/substrate and conductive material layered in the recess (Col. 3-7). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a recess defined by a sidewalls extending into the motherboard to improve the reliability of the interconnection using Hembree's interconnect structure in the APA as cited in claim 5.

Regarding claims 6 and 7, the APA fails to specify the dimensions such as a width and shape of the recessed motherboard contacts being same as a diameter of the solder ball and shape of a semispherical surface of same radius as that of the solder ball respectively. However, as explained above for claim 5, Hembree teaches forming non-reflow electrical contacts between the microelectronic device and a board/substrate comprising a recess defined by inclined sidewalls of the bumps (Fig. 5; Col. 6, line 34-65) or vertical sidewalls (Fig. 5A; Col. 6, line 34-65) extending

into the board/substrate and conductive material layered in the recess (Col. 3-7). The parameters such as length, width, depth, shape/angle of the recessed area, volume of the void in the recess, etc. of the contact pad/area in the chip interconnection technology art are considered to be a matter of design choice to achieve the desired bonding area and interconnect reliabilty. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate width and shape of the recessed motherboard contacts being same as a diameter of the solder ball and shape of a semispherical surface of same radius as that of the solder ball to meet the design and reliability requirements of the interconnect in the APA in view of Hembree as cited in claims 6 and 7 respectively.

The combined teachings of the APA and Hembree apply to Claim 12 as explained above for claim 1.

Regarding claims 13 and 14, the APA discloses compression mechanism/support structure comprising:

- a frame surrounding the substrate
- a backing plate abutting the motherboard
- a thermal plate extending over the frame and adjacent the substrate second surface, and
- a plurality of retention devices comprising a plurality of bolts and nuts extending through the backing plate, frame and thermal plate.

Regarding claim 15, the APA discloses the substrate comprising a microelectronic device package including a microelectronic device attached to and in electrical contact with a first surface of an interposer and wherein the substrate first contact comprises contacts on a second surface of the interposer substrate.

Regarding claim 16, the APA fails to specify using a resilient spacer extending between the thermal plate and the interposer substrate. Hembree teaches using a resilient elastomeric spacer ring/washer spring (22 in Fig. 2; Col. 4, line 4) extending between the thermal plate and the microelectronic device/interposer substrate to enhance the support/compression mechanism. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a resilient spacer extending between the thermal plate and the interposer substrate to enhance the support/compression mechanism using Hembree's structure in the APA as cited in claim 16.

Claim 23 is rejected as explained above for claims 5 and 1.

Claim 25 is rejected as explained above for claims 23, 6, 5 and 1.

The combined teachings of the APA, Hembree and Akram apply to Claim 28 as explained above for claims 1, 5-7 and 23, 25-27.

Claims 29-31 are rejected as explained above for claims 1; 5-1; 7 respectively.

The combined teachings of the APA, Hembree and Akram apply to Claim 32 as explained above for claims 23, 7, 1.

Regarding claim 33, as explained above for claims 23, 7 and 1, the APA in view of Hembree teaches a substrate non-reflow electrical contact comprising a recess defined by sidewalls (vertical and inclined) extending into the motherboard and conductive material layered in the recess but fails to specify using a resilient material disposed between the substrate and the conductive material layer. It is conventional in the chip interconnection technology art to use additional resilient material/layers under conductive material layer to improve the interconnection reliability. Akram teaches using soft/resilient materials such as gold, etc. (Fig. 3c and 3d; Col. 6, line 13) between the substrate and conductive material/layers to improve the interconnect reliability. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a resilient material disposed between the substrate and the conductive material layer to improve the interconnect reliability using Akram's structure in the APA in view of Hembree as cited in claim 33.

Response to Arguments

3. Applicant's arguments filed on 01-02-01 have been fully considered but they are not persuasive.

A. Applicant contends that Hembree's non-reflow electrical contacts/design do not apply to the microelectronic component assembly as claimed. However, the assembly processes, bonding methods and materials used in assembly and fabrication of Hembree's microelectronic components for functional testing and certification of a known good die of a package are those used in the conventional fabrication and assembly of microelectronic devices in chip packaging and interconnection technology art (Col. 3-8). Therefore, Hembree's non-reflow electrical contacts design/teaching is applied to the APA.

B. Applicant contends that Akram's reference do not disclose using resilient material layers under the conductive material layer. However, as explained above for claim 27, Akram teaches using a multitude of metal layers including soft/resilient materials such as gold, etc. (Fig. 3c and 3d; Col. 6, line 13) between the substrate and conductive material/layers to improve the interconnect reliability.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted directly to Art Unit 2811 by Facsimile transmission. Papers should be faxed to Art Unit via Tech Center 2800 fax center located in Crystal Plaza 4, Room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh at (703) 305-3410. The examiner can normally be reached on Monday-Friday from 08:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

03-18-01

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER